Remarks

Claims 1-6 have been rejected under 35 U.S.C. §102(b) as being anticipated by Ikeda (US 6,240,244). This rejection is respectfully traversed and submitted to be inapplicable to the claims for the following reasons.

Ikeda discloses a video disk apparatus including a controller 23, a switching section 15, a recording buffer memory 14 and a reproduction buffer memory 19. The apparatus is capable of simultaneous recordation and reproduction of digital video data to and from a medium 18. During operation, video data is continuously written into the recording buffer memory 14 and intermittently read from the recording buffer memory 14 and recorded on the medium 18 in a sequential manner. While the video data is being read from the recording buffer memory 14, the controller 23 controls the switching section 15 such that the video data is supplied to the medium 18. Since the video data is only intermittently read from the recording buffer memory 14, the period of time when the video data is not being read from the recording buffer memory 14 can be used for the reproduction of data previously stored on the medium 18. During this reproduction period, the controller 23 controls the switching section 15 such that the data reproduced from the medium 18 is sequentially stored in the reproducing buffer memory 19 from which it is eventually read and displayed on a monitor 21. (See column 5, line 6 - column 6, line 67 and Figure 1).

As discussed above, the apparatus of Ikeda is capable of performing simultaneously processes of recording and reproducing digital video data and utilizes the recording buffer memory 14 and the reproducing buffer memory 19, respectively, when performing these operations. However, it is also apparent that the types of accesses to the recording buffer memory 14 and the reproducing buffer memory 19 are all sequential and the apparatus of Ikeda fails to disclose or suggest, for example, random accessing being associated with one of the recording buffer memory 14 and the reproducing buffer memory 19. On the other hand, the present invention, as recited in claim 1, recites that the file system includes a plurality of internal buffers for temporarily holding data transferred between a plurality of processors and a hard disk, the plurality of internal buffers being for respective kinds of accesses to a same file executed at a same time between the plurality of processors and the hard disk. Therefore, the present invention as recited in claim 1 allows for access to the data to be a dynamic random access when viewed from the file system. In the random access to the data, that

the data is stored in an internal buffer as opposed to the hard disk is beneficial for reducing the load on the hard disk. It is apparent that Ikeda fails to disclose or suggest this feature as recited in claim 1.

Because of the above-mentioned distinctions, it is believed clear that claims 1-6 are allowable over Ikeda. Furthermore, it is submitted that the distinctions are such that a person having ordinary skill in the art at the time of invention would not have been motivated to modify Ikeda or make any combination of the references of record in such a manner as to result in, or otherwise render obvious, the present invention as recited in claim 1-6. Therefore, it is submitted that claims 1-6 are clearly allowable over the prior art of record.

In view of the above remarks, it is submitted that the present application is now in condition for allowance. The Examiner is invited to contact the undersigned by telephone if it is felt that there are issues remaining which must be revolved before allowance of the application.

Respectfully submitted,

Tetsuya SUZUKA

Bv:

David M. Ovedovitz Registration No. 45,336 Attorney for Applicant

DMO/jmj Washington, D.C. 20006-1021 Telephone (202) 721-8200 Facsimile (202) 721-8250 August 16, 2006